The listing of Claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A phase changeable memory device comprising:

an integrated circuit substrate;

a first storage active region on the integrated circuit substrate having a first width;

a second storage active region on the integrated circuit substrate having a second width; and

a transistor active region on the integrated circuit substrate between the first and second storage active regions, the first and seconds widths being less than a width of the transistor active region.

2. (Original) A device according to Claim 1 wherein the first width is equal to the second width and the first and second widths are about half of the width of the transistor active region.

3. (Original) A device according to Claim 1 further comprising a plurality of gate lines defining a plurality of rows of the phase changeable memory device, wherein a plurality of the first and second storage active regions are disposed alternately along the rows in a region between first and second gate lines of the plurality of gate lines and wherein the widths of the first and second storage active regions and the width of the transistor active region are parallel to the plurality of gate lines.

4. (Original) A device according to Claim 1 wherein the transistor active region comprises first and second sidewalls extending from a first end of the transistor active region to a second end of the transistor active region, wherein the first storage active region protrudes from the first sidewall of the transistor active region at the first end of the transistor

active region and wherein the second storage region protrudes from the second sidewall of the transistor active region at the second end of the transistor active region.

5. (Original) A device according to Claim 1 wherein the transistor active region is a first transistor active region, the device further comprising:

a second transistor active region; and

a connector active region between the first transistor active region and the second transistor active region that electrically couples the first and second transistor active regions.

6. (Original) A device according to Claim 1 further comprising:

a first data storage element on the first storage active region;

a second data storage element on the second storage active region;

a first lower plug that electrically couples the first data storage element to the first storage active region; and

a second lower plug that electrically couples the second data storage element to the second data storage region.

7. (Original) A device according to Claim 6 further comprising:

a plurality of bit lines on the integrated circuit substrate;

a first upper plug that electrically couples a first bit line of the plurality of bit lines to the first data storage element; and

a second upper plug that electrically couples a second bit line of the plurality of bit lines to the second data storage element.

8. (Original) A device according to Claim 7:

wherein the first data storage element comprises a first barrier pattern that is electrically coupled to the first lower plug and a first phase changeable material pattern on the first barrier pattern;

wherein the second data storage element comprises a second barrier pattern that is electrically coupled to the second lower plug and a second phase changeable material pattern on the second barrier pattern; and

wherein the first and second upper plugs comprise heater plugs that generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

9. (Original) A device according to Claim 8 wherein a diameter of the first lower plug is larger than a diameter of the first upper plug and wherein a diameter of the second lower plug is larger than a diameter of the second upper plug.

Claims 10-11 (Canceled).

12. (Original) A device according to Claim 7:

wherein the first data storage element comprises a first phase changeable material pattern that is electrically coupled to the first lower plug and a first barrier pattern on the first phase changeable material pattern;

wherein the second data storage element comprises a second phase changeable material pattern that is electrically coupled to the second lower plug and a second barrier pattern on the second phase changeable material pattern; and

wherein the first and second lower plugs comprise heater plugs that generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

13. (Original) A device according to Claim 12 wherein a diameter of the first lower plug is less than a diameter of the first upper plug and wherein a diameter of the second lower plug is less than a diameter of the second upper plug.

14. (Currently Amended) A device according to Claim ~~12~~ 7 further comprising:

a common source interconnection on the integrated circuit substrate; and

a common source plug that electrically couples the common source interconnection to the transistor active region.

15. (Original) A device according to Claim 14 further comprising an interlayer dielectric on the integrated circuit substrate, wherein the common source plug is disposed in the interlayer dielectric and wherein the common source interconnection is disposed in the interlayer dielectric on the common source plug.

16. (Original) A device according to Claim 1 further comprising:

a first data storage element on the first storage active region;

a second data storage element on the second storage active region;

first and second lower plugs on the integrated circuit substrate;

a first buffer pattern on the first lower plug;

a second buffer pattern on the second lower plug;

a first intermediate plug on the first buffer pattern that electrically couples the first data storage element to the first storage active region; and

a second intermediate plug on the second buffer pattern that electrically couples the second data storage element to the second data storage region.

17. (Original) A device according to Claim 16 further comprising:

a plurality of bit lines on the integrated circuit substrate;

a first upper plug that electrically couples a first bit line of the plurality of bit lines to the first data storage element; and

a second upper plug that electrically couples a second bit line of the plurality of bit lines to the second data storage element.

18. (Original) A device according to Claim 17:

wherein the first data storage element comprises a first barrier pattern that is electrically coupled to the first intermediate plug and a first phase changeable material pattern on the first barrier pattern;

wherein the second data storage element comprises a second barrier pattern that is electrically coupled to the second intermediate plug and a second phase changeable material pattern on the second barrier pattern; and

wherein the first and second upper plugs comprise heater plugs that generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

Claims 19-20 (Canceled).

21. (Original) A device according to Claim 17:

wherein the first data storage element comprises a first phase changeable material pattern that is electrically coupled to the first intermediate plug and a first barrier pattern on the first phase changeable material pattern;

wherein the second data storage element comprises a second phase changeable material pattern that is electrically coupled to the second intermediate plug and a second barrier pattern on the second phase changeable material pattern; and

wherein the first and second intermediate plugs comprise heater plugs that generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

22. (Currently Amended) A device according to Claim ~~21~~ 16 further comprising:

a common source interconnection on the integrated circuit substrate; and

a common source plug that electrically couples the common source interconnection to

the transistor active region.

23. (Currently Amended) A device according to Claim ~~23~~ 22 further comprising an interlayer dielectric on

the integrated circuit substrate wherein the common source plug is disposed in the interlayer dielectric and wherein the common source plug is dispose on the interlayer dielectric.

Claims 24-46 (Canceled).

47. (Original) A phase changeable memory device comprising:

an integrated circuit substrate;

a first storage active region on the integrated circuit substrate having a first cross sectional area;

a second storage active region on the integrated circuit substrate having a second cross sectional area; and

a transistor active region on the integrated circuit substrate between the first and second storage active regions, the first and seconds cross sectional areas being less than a cross sectional area of the transistor active region.